REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this reply, claims 1-27 will remain in the application.

Specification

The title of the application has been amended as requested.

Claims Rejections - 35 U.S.C. § 102

Claims 1-13, 15-19, 21-25, and 27 were rejected under 35 U.S.C. § 102(b) as allegedly being unpatentable over U.S. Patent No. 5,740,413 to Alpert, et al. ("the Alpert patent" or "Alpert").

Applicants teach a technique for, in one embodiment, causing a programmable processor to process one instruction at a time. Exemplary techniques to perform single-step debugging include taking an exception after each instruction or invoking emulation mode after each instruction. The particular single step debugging technique that is performed may be a function of the state of control bits, or the processor's current operating mode, or both.

The Alpert patent, in contrast, is directed to providing address breakpoints and branch breakpoints; use of these techniques may enable single-stepping. In accord with an aspect of the Alpert patent, a processor includes an address breakpoint unit and a branch breakpoint unit. The processor includes

control bits that may determine whether either, none, or both of these units are enabled.

With respect to independent claim 1, Applicants respectfully submit that Alpert does not disclose or suggest "selecting one of a plurality of debugging modes as a function of a current operating mode of a processor" as recited in claim 1. Alpert does describe enabling debug events during execution of operating system and non-operating system routines. Although Alpert describes more than one operating mode for the processor, Alpert does not disclose a plurality of debugging modes, since Alpert's debugging events are not disclosed as being debugging modes.

In addition, Alpert does not teach or suggest selecting one of multiple debugging modes as a function of the processor's current operating mode. In Alpert, different debug events may occur in different operating modes, but Alpert does not disclose any dependency of a selection of debugging events on the processor's current operating mode.[1]

Moreover, Applicants note that the Alpert patent mentions the effect of certain control bits on the "enablement of the debug events," col. 8, ll. 51-52 (emphasis added). Control bits determine whether the address breakpoint unit and the branch breakpoint unit are enabled or disabled. When a particular breakpoint unit is enabled, it allows the respective breakpoint debug event to be handled. Thus, if the address breakpoint unit

[1] This argument is not intended to concede that debugging events are equivalent to debugging modes, or that Alpert anticipates the "selecting" limitation. Rather, it is intended to illustrate that Alpert does not disclose the limitation of "as a function of the current operating mode of a processor."

is enabled, then the debug event that is generated upon reaching the breakpoint address will be processed. The branch breakpoint unit acts in an analogous way.

This is different from the subject matter of claim 1. While Alpert discusses the "enablement" of debug events, claim 1 recites "selecting" a debugging mode. Alpert's enablement of debug events is a passive process in which debug events are merely permitted to occur by the enablement of the appropriate breakpoint unit. In contrast, "selecting one of a plurality of debugging modes" involves an active process. Also, as discussed above, the "debug events" of Alpert are not equivalent to the "debugging modes" or "mode of debugging" in the current application. Accordingly, Alpert does not disclose or suggest the subject matter of claim 1.

With respect to independent claims 5, 11, 17, and 22, Applicants respectfully submit that Alpert does not teach or suggest the claimed subject matter. For the same reasons as discussed above with respect to claim 1, Alpert does not disclose the selection of a debugging mode. In addition, for the same reasons as discussed above with respect to claim 1, Alpert does not disclose selecting one of a plurality of debugging modes. Accordingly, Alpert does not disclose or suggest the subject matter of claims 5, 11, 17, and 22.

Furthermore, for the same reasons as discussed above with respect to claim 1, Alpert does not disclose the selection of "one of a plurality of debugging modes as a function of the current operating mode of the processor" as recited in claim 17. Thus, Alpert does not disclose the subject matter of claim 17.

For at least these reasons, Alpert does not disclose or suggest the subject matter of independent claims 1, 5, 11, 17, and 22, and these claims are believed to be allowable. Claims 2-4, 6-10, 12-13, 15-16, 18-19, 21, 23-25, and 27 depend from independent claims that are believed to be allowable. For at least this reason, the rejections relating to these claims are respectfully traversed.

Claim Rejections - 35 U.S.C. § 103

Claims 14, 20, and 26 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,530,804 to Edgington, et al.

These claims depend from claims that are believed to be allowable, as discussed above. For at least this reason, claims 14, 20, and 26 are believed to themselves be allowable, and the rejections relating to these claims are respectfully traversed.

Conclusion

Applicant respectfully asks that all claims be allowed. No fees are believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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